REMARKS

Claims 1-70 are currently pending, claims 1-17, 52-55, and 67-70 stand rejected, and claims 18-51 and 56-66 are withdrawn. Claims 1, 8, 13, 52, and 67 have been amended. No new matter has been included. Applicants reserve the right to pursue original and other claims in this and in other applications.

Applicants appreciate the Examiner's time and attention during a telephonic conference on April 4, 2007 with Applicants' representative. During the conference, Examiner Giles identified the elements of Kole (U.S. Pat. No. 6,501,064)("Kole") that allegedly correspond to elements of the claimed invention. Examiner Giles indicated that:

- Kole's element 71 (FIG. 4B) corresponds to first and second voltages of claim 1.
- Kole's element 30 (FIG. 4B) corresponds to element 186 (FIG. 7) of the claimed invention.
- Kole's intersection of lines between elements 20, 30, and S1 (FIG. 4B) corresponds to element A (FIG. 7) of the claimed invention.
- in Kole, an inactive signal corresponds to a Ground voltage or Ground potential.

Claims 1-2, 4, 6-9, 11-14, 16, 52-53, 55, 67-68, and 70 stand rejected under 35 U.S.C. 102 (e) as being anticipated by Kole. Applicants respectfully traverse this rejection.

Claim 1 recites an image array pixel comprising "a charge sharing node; a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to first and second voltage sources for providing first and second voltages, respectively, the other of said source/drain regions being coupled to said node; and a row select transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to the first and second voltages, the gate of said row select transistor being coupled to a third voltage source, said third voltage source being different from said first and second voltage sources, wherein the gate of said reset transistor is coupled to a fourth voltage source being different from said first, second, and third voltage sources."

Kole discloses:

> An image pick-up [that] includes a number of active sensor elements ...arranged in an array and a number of conductive lines extending over the surface of the array for the transfer of supply and signals. Each sensor element includes a light sensor (20) and an amplifier. According to the invention, a reduction in the number of lines can be achieved while functionality is maintained. In a first and a second embodiment (11; 12), a sensor element includes a first switch (S1) associated with the sensor and a second switch (S2; S3) associated with the amplifier, the switches being controlled by a common control signal. In a third embodiment (13), a sensor element includes a series arrangement of a first switch (S1) and a second switch (S2) included between the sensor and a supply line. In a fourth embodiment (14), a select signal is also used as a supply for the amplifier.

(Kole, Abstract)

Kole, however, fails to disclose or suggest a gate of a row select transistor being "coupled to a third voltage source" and a gate of a reset transistor is "coupled to a fourth voltage source." As such, the rejection of claim 1 should be withdrawn and the claim and its dependant claims 2-7 allowed.

Claim 8 recites a pixel circuit, comprising "a photo sensor; a storage node for receiving charges from said photo sensor; a reset transistor for resetting said storage node, said reset transistor being switchably coupled to a first and second voltage level, a gate of said reset transistor being coupled to a reset control line; and a row select transistor being switchably coupled to said first and second voltage level, a gate of said row select transistor being coupled to a row select control line."

Kole fails to disclose or suggest "a gate of said reset transistor being coupled to a reset control line" and "a gate of said row select transistor being coupled to a row select control line." As such, the rejection of claim 8 should be withdrawn and the claim and its dependant claims 9-12 allowed.

Claim 13 discloses an image array pixel comprising "a charge storing node; a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node, the gate of said reset transistor being coupled to a reset

control line; a row select transistor being switchably coupled to said first and second voltage level, a gate of said row select transistor being coupled to a row select control line; and a source-follower transistor having source/drain regions on opposite sides of a gate of said source-follower transistor, one of said source/drain regions of said source-follower transistor being coupled to said first and second voltage and to said one of said source/drain regions of said reset transistor."

Kole fails to disclose or suggest a "gate of said reset transistor being coupled to a reset control line" and "a gate of said row select transistor being coupled to a row select control line." As such, the rejection of claim 13 should be withdrawn and the claim and its dependant claims 14-17 allowed.

Claim 52 discloses a processing system, comprising "a processor; an imager array coupled to said processor, one pixel of said image array comprising: a charge sharing node; a row select transistor being switchably coupled to said first and second voltage, a gate of said row select transistor being coupled to a row select control line; and a reset transistor having source/drain regions on opposite sides of a gate of said reset transistor, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node, the gate of said reset transistor being coupled to a reset control line."

Kole fails to disclose or suggest a "gate of said row select transistor being coupled to a row select control line" and a "gate of said reset transistor being coupled to a reset control line." As such, the rejection of claim 52 should be withdrawn and the claim and its dependant claims 53-55 allowed.

Claim 67 discloses an imaging device, comprising "a processor; an imager array coupled to said processor, one pixel of said image array comprising: a charge sharing node; a row select transistor being switchably coupled to a first and second voltage, a gate of said row select transistor being coupled to a row select control line; and a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to said first and second voltage, the other of said source/drain regions being coupled to said node, a gate of reset transistor being coupled to a reset control line."

Kole fails to disclose or suggest a "gate of said row select transistor being coupled to a row select control line" and a "gate of reset transistor being coupled to a reset control line."

As such, the rejection of claim 67 should be withdrawn and the claim and its dependant claims 68-70 allowed.

Claims 3, 5, 10, 15, 17, 54, and 69 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Kole. Applicants respectfully traverse this rejection.

Claims 3 and 5; 10; 15 and 17; 54; and 69 respectively depend from claims 1; 8; 13; 52; and 67 and are allowable over Kole for at least the reasons noted above.

Additionally, the Examiner's Official Notice, which Applicants respectfully traverse, using ground potential for an inactive signals does not overcome the shortcomings of Kole noted above with respect to claims 3, 10, 15, 54, and 69. Examiner's Official Notice of the use of pixels that don't receive any light during a reset, which Applicants respectfully traverse, does not overcome the shortcomings of Kole noted above with respect to claims 5 and 17. As such, the rejection of claims 3, 5, 10, 15, 17, 54, and 69 should be withdrawn and the claims allowed over Kole and Official Notice.

In view of the above, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

By _____ reg # 41,191

Thomas J. D'Amico
Registration No.: 28,371
Michael A. Weinstein
Registration No.: 53,754
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicants